PAN AFRICA CHRISTIAN UNIVERSITY

BACHELOR OF BUSINESS INFORMATION TECHNOLOGY AND BACHELOR OF SCIENCE IN INFORMATION TECHNOLOGY

END OF TERM EXAMINATION

DEPARTMENT: **COMPUTING & INFORMATION TECHNOLOGY**

COURSE CODE: **BSIT 206**

CAMPUS: **ROYSAMBU**

COURSE TITLE: **COMPUTER ORGANIZATION AND ARCHITECTURE**

EXAM DATE: **THURSDAY,XXXX,APRIL ,2026**

TIME: **2:00PM -4:00PM**

INSTRUCTIONS

- This exam script has **TWO (2)** sections.
- Read all questions carefully before attempting.
- Answer All questions in Section **A** and any other THREE questions in Section **B.**
- Write only your **student number** on the answer booklet provided.

SECTION A (Answer ALL questions)

QUESTION ONE (20 Marks) Compulsory

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a) During routine system upgrades, laboratory computers experience performance slowdowns due to frequent memory access delays. Analyze THREE limitations of the von Neumann architecture that may contribute to this problem. [6 Marks]
b) Explain what handshaking mechanisms are in I/O communication. Provide THREE examples of handshaking techniques used between devices [6 Marks]
c) A keyboard sends characters to a computer at irregular intervals, while the CPU processes data at a fixed rate.

i. Explain how buffering helps in this situation [2 Marks]
ii. describe TWO types of buffering techniques that can be used. [4 Marks]

d) Differentiate between SRAM and DRAM [2 Marks]

QUESTION TWO (15 Marks)

a)Describe computer architecture and briefly outline its scope in the design and evaluation of modern computer systems. [4 Marks]
b) Assume the cache can store several blocks of memory at a time, and different strategies are used to decide where a memory block is placed in the cache. Using this context, explain the following cache mapping techniques, showing how each technique determines the location of a memory block in the cache:
i. Direct mapping
ii. Associative mapping
iii. Set-associative mapping [6 Marks]
c) Differentiate RISC with CISC architecture [5 Marks]

QUESTION THREE (15 Marks)

a) In a multiprocessor system, maintaining data consistency is critical. Explain the cache coherence problem and describe why cache coherence mechanisms are necessary. [5 Marks]

b) Differentiate between the von Neumann and Harvard architectures by explaining THREE key differences relevant to system performance and design. [6 Marks]
c)Explain what Instruction-Level Parallelism (ILP) is and how it improves CPU performance [4 Marks]

QUESTION FOUR (15 Marks)

a) Modern computer systems are developed using multiple levels of abstraction. Explain FOUR levels and justify their importance in the design and management of complex computer systems.
[4 Marks]
b) Explain THREE reasons why memory interleaving is beneficial in high-performance computer systems.
[6 Marks]

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c) Explain the following memory performance metrics and analyze how each affects overall system performance:
i. Memory latency
ii. Cycle time
iii. Bandwidth [3 Marks]
d)Compare DMA-based transfer with programmed I/O [2 Marks]

QUESTION FIVE (15 Marks)

b) When executing a program, the CPU follows a defined sequence of operations. Explain the instruction execution cycle, identifying the purpose of each stage. [6 Marks]

d) Despite its performance benefits, pipelining introduces several challenges. Discuss THREE pipeline hazards and explain techniques used to minimize their impact in modern processors. [6 Marks]

b) Explain RAID levels 0, 1, and 5, describing how each level stores data and provides performance or redundancy. [3 Marks]

QUESTION SIX (15 Marks)

a) A student runs several applications simultaneously on a laptop with limited physical memory. Define virtual memory and explain THREE benefits it provides in this situation. [6 Marks]

b) The operating system manages memory using paging and segmentation. Explain how paging and segmentation operate, highlighting how each technique manages memory allocation. [6 Marks]

c) During periods of heavy system usage, page faults increase significantly. Analyze THREE page replacement algorithms, explaining how each selects a page for replacement. [3 Marks]

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